Mitigation of harmonics in a grid system with sliding mode fractional order controller integrated UPQC

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Abstract—

In recent times, the UPQC has been developed as a FACTS controller for weak buses and buses with non-linear loads. The UPQC can improve the voltage at the receiving end and provide harmonic compensation to the source current. The recommended closed-loop UPQC module is to augment the dynamic response of the UPQC system using an SMFOPI controller. Simulink replicas have been extended for PI and SMFOPI-controlled UPQC frameworks. The results of the PI and SMFOPI-based UPQC module show that the voltage retaliation of FOPI is superior to the outcome of the PI controlled UPQC system. The investigation denotes that the SMFOPI UPQC module has a reduced settling time, steady-state error and harmonics.

Keywords: Active filters, Dynamic Voltage Restorer, ‘’UPQC’’, Total Harmonic Distortion, Wind Generator.

I. INTRODUCTION

The goal of an electric power system is to provide its clients with a smooth and stable sinusoidal voltage with consistent magnitude and frequency. Electricity generators produce a signal that is very close to a sinusoidal waveform. However, designing and operating industrial and commercial power systems requires a thorough analysis to evaluate the system's initial and future performance, reliability, safety, and capacity to meet production and operational requirements.

Sometimes, distorted waveforms are analysed to investigate the harmonious components of the wave patterns. Voltage and current waveforms can be distorted by nonlinear loads, which are common in the power system. With the increasing use of nonlinear loads in modern power systems, it has become essential to establish criteria to prevent power quality problems, such as decreased system efficiency, low power factor, malfunctioning electronic devices, and reduced equipment lifespan.

Harmonic currents produced by DC loads can distort the voltage waveform and damage other loads in the system. To address this issue and protect the loads from distortion, the harmonic components of the voltage and current must be compensated. Although inactive filters can reduce the problem, they have several drawbacks, such as fixed compensation, larger size, and resonance issues.

To overcome these difficulties, Static Active Filters (SAF) have been used with inactive filters, but this method does not reduce the potential for harmonics. The Unified Power Quality Conditioner (UPQC) has been developed to handle voltage and current harmonic effects simultaneously. The UPQC framework consists of two dynamic power channels connected in series and parallel with a common DC link. The series capacitor provides voltage harmonic containment and isolation, and the shunt capacitor controls current harmonics.

This paper presents a comprehensive evaluation of UPQC. A two-bus system with and without UPQC is presented, and a comparative analysis of simulation results is provided. The basic model of UPQC is shown in Figure 1.

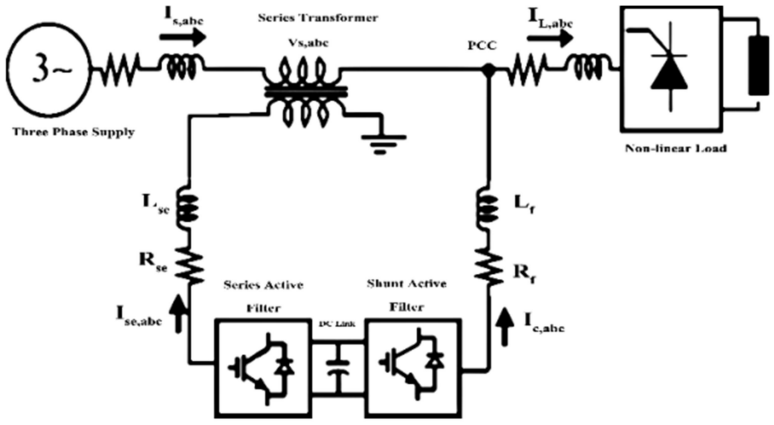

Figure 1: UPQC configuration

The basic arrangement of the 'UPQC' involves two voltage source inverters. The first inverter is used as an arrangement APF and the second one is used as a shunt APF. They are connected consecutively through a DC interface capacitor. The arrangement APF is connected to the source and purpose of association using three single-stage arrangement transformers. It has the ability to compensate for voltage THD, voltage flicker, and improve voltage regulation. To eliminate the high switching ripple contented in the series APF infused voltage, a low-pass aptitude capacitor filter is integrated diagonally to the derivative of each series transformer.

The shunt APF has the ability to suppress the current THD, compensate for reactive power, offset arrangement present, and control the DC interface voltage among APFs equally. To remove the high exchanging swell experienced in the shunt APF infused current, the SAPF is

connected during a little evaluated limit inductive channel. Yong provided a synchronized control approach for 'UPQC' in a 3-stage, 4-wire framework. Khadkikar improved Electric PQ using 'UPQC'.

II. UPQC CONTROL MODULES

The UPQC design comprises a series APF, a shunt APF, and a mutual DC link. Figure 1 shows a simple configuration of a typical UPQC. The series active power filter proposed in [14] isolates harmonics between the transmission and distribution systems, mitigating sag, swell, and THD at PCC. Meanwhile, current harmonics are compensated by the shunt APF [15]. The DC link regulates the DC voltage between the two filters [14].

The UPQC circuit is composed of two voltage source bidirectional converters with a shared DC bus, linked back-to-back via IGBTs. One inverter is connected in series with the load, while the other is in shunt. The shunt inverter works as a current source for injecting compensating current ish, while the supply side inverter, connected in series with the load, serves as a voltage source, supplying Vsc through an insertion transformer.

The Conventional control technique uses the "p-q theory" for the shunt APF and the hysteresis band controller transforming the Park transformation or dq0 for the Series APF. In this paper, P.Q of the system has been enhanced with the use of UPQC. The Series APF reduces voltage sags and swells at the load end by adding a voltage that is in line with the supply. Control activity is on the order of 2 msec, guaranteeing a stable voltage supply even under oscillation conditions. The most important aspect of a Series-APF is the protection of sensitive loads from voltage sags/swells arriving from the system.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} = \sqrt{3/2} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{s,a} \\ v_{s,b} \\ v_{s,c} \end{bmatrix} \quad (1)$$

The Series-APF is specifically designed to handle critical loads. In the event of a fault occurring on another line, the load is compensated to its pre-fault value by inserting series voltage. The magnitudes of the three inserted phase voltages are restricted in a way that decimates any harmful effects of a bus fault on the load voltage. The design of Series APF is based on the concept of a single vector model (SVM) as presented in [13]. SVM is derived from the distorted supply. The general configuration of Series APF is illustrated in Figure 2.

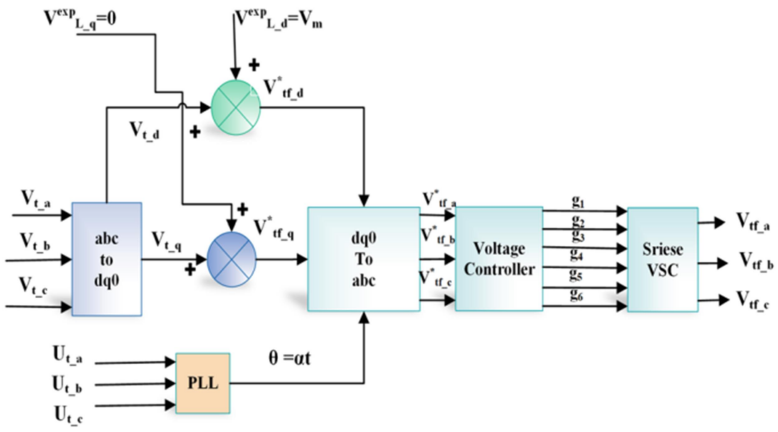

Figure 2: Control structure of series filter

Fig. 3 illustrates the general configuration of a shunt-APF. Its main function is to filter equal but opposing harmonic compensatory current to compensate for load current harmonics. Essentially, a shunt-APF acts as a current source, filtering the load's harmonics with a 180-degree phase shift. It is mainly used as a voltage regulator and a harmonic neutralizer between the nonlinear load and the consumer side source. The shunt-APF is controlled using the p-q hypothesis, and the modelling equations are used to convert 3-phase voltages and currents from abc to dq coordinates.

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \sqrt{3/2} \begin{vmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{vmatrix} \begin{bmatrix} i_{s,a} \\ i_{s,b} \\ i_{s,c} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_{cd,r} \\ I_{cq,r} \end{bmatrix} = 1/v_\alpha^2 + v_\beta^2 \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} -\bar{P} + P_0 + \bar{P_{Loss}} \\ -Q \end{bmatrix} \quad (3)$$

Real and reactive components are getting from the given in Eq. (4). Since Real and reactive components are a relation of V and I

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_d & v_q \\ -v_q & v_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (4)$$

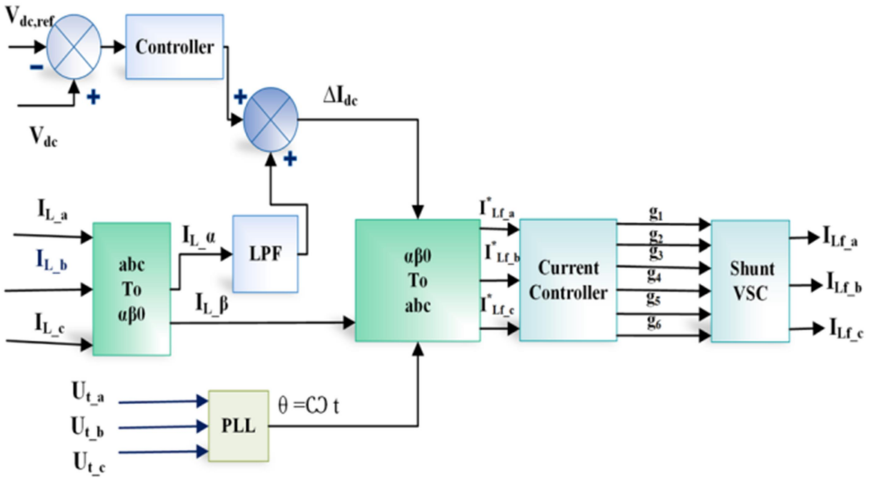

Figure 3: Control structure of series filter

In a three-phase system, deliberate reference signals are used to alter neutralized, harmonic, and sensitive currents in the load. The HCC algorithm [16] is employed to generate a switch signal by comparing the existing signal with the reference signal. The performance of the UPQC is improved based on the acceleration and quality of the reference signal.

III. SMFO-PI CONTROLLER CONFIGURATION

Fractional-order calculus has been utilized in the design of fractional-order controllers as an improvement over the conventional PID, by incorporating fractional-order parameters to increase the degrees of freedom in control. In the time domain, the equation for the fractional-order controller can be expressed as shown in Eq. (5).

$$U_{FO\text{-}PID}(t) = K_p e(t) + K_i \frac{d^{-\lambda} e(t)}{dt^{-\lambda}} + K_d \frac{d^{\mu} e(t)}{dt^{\mu}} \quad (5)$$

In control theory, PID (proportional-integral-derivative) controllers are widely used to regulate processes. The controller has three parameters, namely proportional gain Kp, integral gain Ki, and derivative gain Kd. The error at different time instances is given by e(t). In contrast, fractional-order controllers have two additional parameters, λ and μ, resulting in two additional degrees of freedom. This makes the fractional-order controller perform better than the PID controller. When the Laplace transform of the fractional-order controller's equation (Eq. 5) is taken, it results in the behavior of an FO-PID controller, which is described in Eq. 6 in the s-domain.

$$U_{FO\text{-}PID}(s) = K_p + K_i \frac{1}{s^{\lambda}} + K_d s^{\mu} E(s) \quad (6)$$

Fig. 4 shows the block diagram of the FO-PID controller used in this work, where Kp, Ki, and Kd are the gains of the controller and E(s) represents the Laplace transform of the error, as defined in Eq. (6).

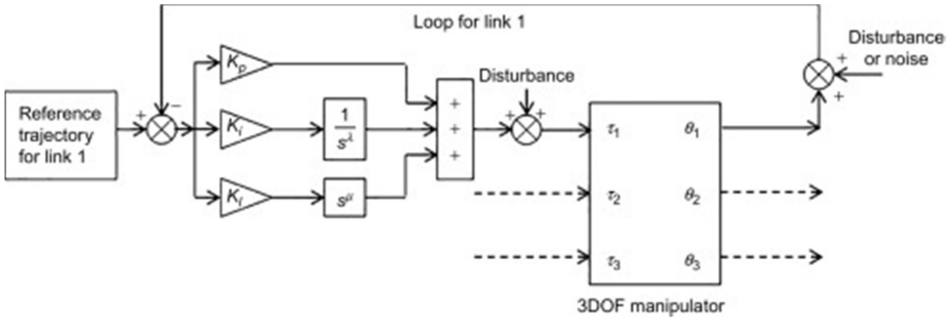

Figure 4: FO-PI controller structure

All classical PID-controllers are specific cases of the fractional PIλDμ-controller. However, the PIλDμ-controller is more flexible and allows for better adjustment of the dynamic properties of a fractional-order control system.

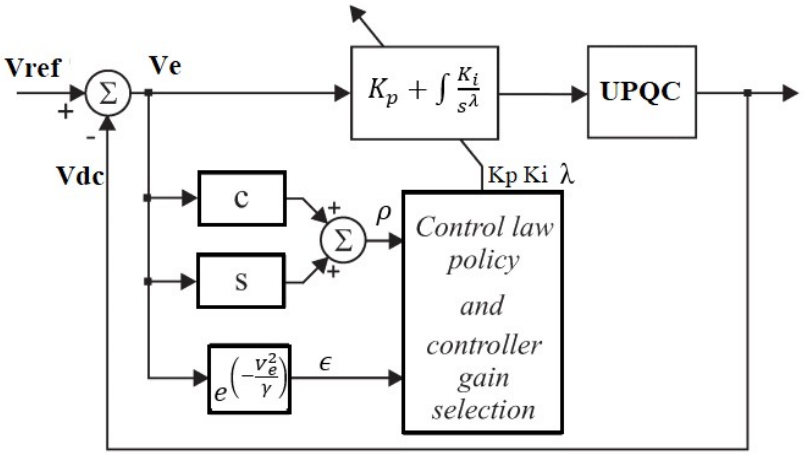

Figure 5: Sliding mode FO-PI controller structure

As per the control law policy the value of the fractional order is varied as per the given equation (7).

$$\lambda = \frac{1}{e^{V_e}} \qquad (7)$$

The λ is adjusted as per the error value generated by the DC link voltage comparison with a reference value. The updated controller in the shunt module is integrated into the UPQC and a comparative analysis is carried out in the next section with simulation results.

IV. SIMULATION RESULTS

In this section, we will evaluate the performance of the UPQC control system using numerical simulations in the MATLAB/Simulink environment. Our primary quality goals are to maintain minimum error and ripple of the VDC voltage of the DC intermediate circuit, as shown in Figure 6, and to minimize the current and voltage THD. We will assess these goals under two conditions: a linear load and a highly polluting nonlinear load in terms of harmonic content.

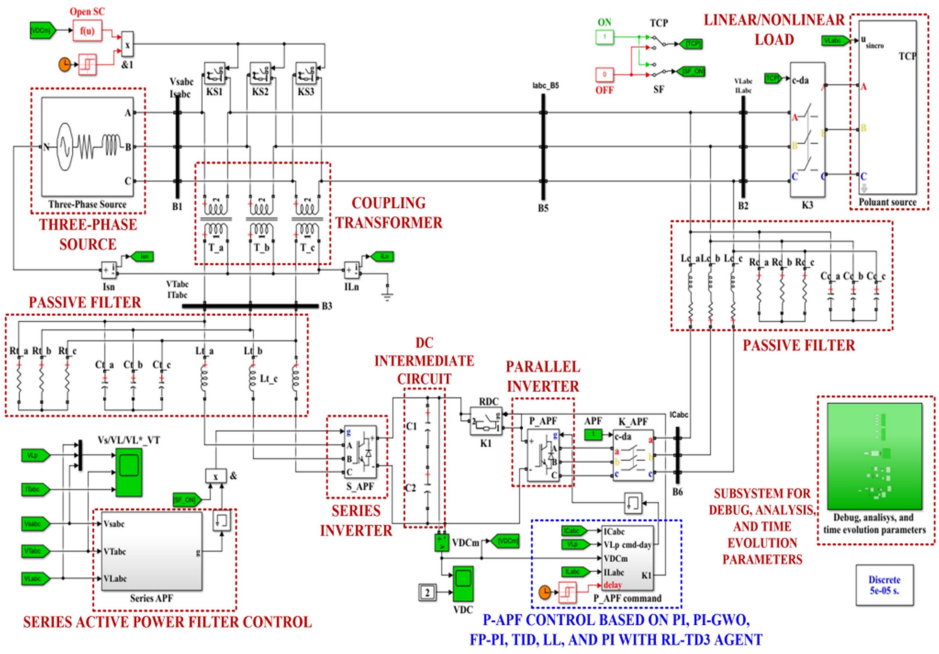

Figure 6: UPQC modeling connected to 3-ph grid

In the MATLAB/Simulink implementation of the UPQC system, various components are used. These include a three-phase source block, passive filter blocks, active series filter and APF control subsystems, series and parallel inverter blocks, coupling transformer blocks, DC intermediate circuit block, nonlinear/linear load, and time evolution for the UPQC system parameters subsystem. The nonlinear load comprises a controlled inverter, which consists of an RL series circuit at the output, with a resistance of 4 ohms and an inductance of 35 mH. The main objective of the UPQC system is to enhance the power quality on both the source and load sides. The subsystem for controlling active filters typically uses classical PI controllers.

The simulation is done with sags and swells created between 0.2-0.4sec and 0.6-0.8sec respectively in a simulation time of 1sec. The below figure 7 graphs are the source voltage, load voltage, series filter injected voltage and frequency of the load.

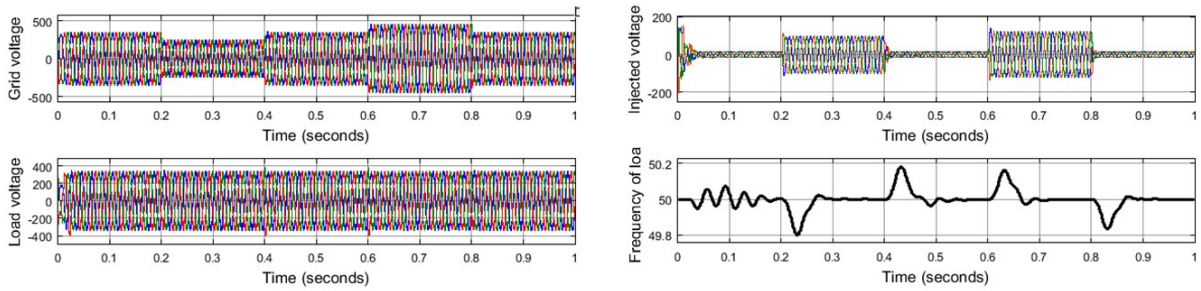

Figure 7: Voltage and frequency profiles of the grid system

For the same operating conditions, the current profiles of the source, load and compensation current along with DC link voltage of the UPQC module can be observed in figure 8 below.

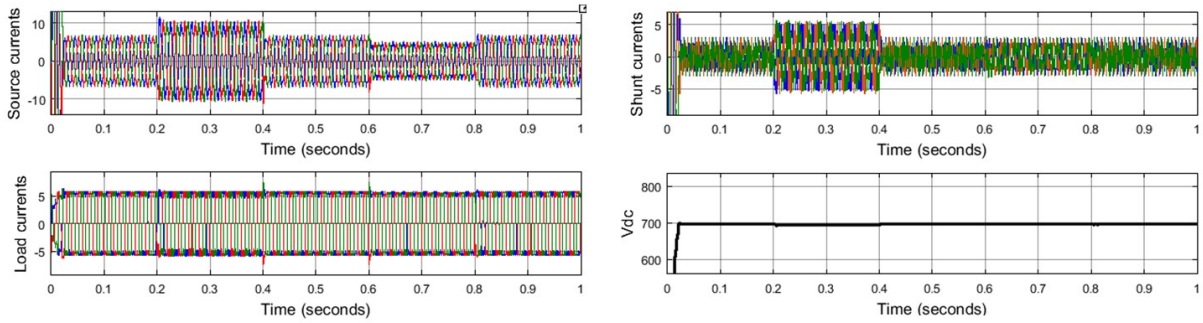

Figure 8: Current and DC link voltage profile of the grid system

The source current of phase A for every controller (PI, FOPI and SMFOPI) are analysed using FFT analysis tool in 'powergui' for calculating THD. The THDs of the analysed signal are presented in figure 9.

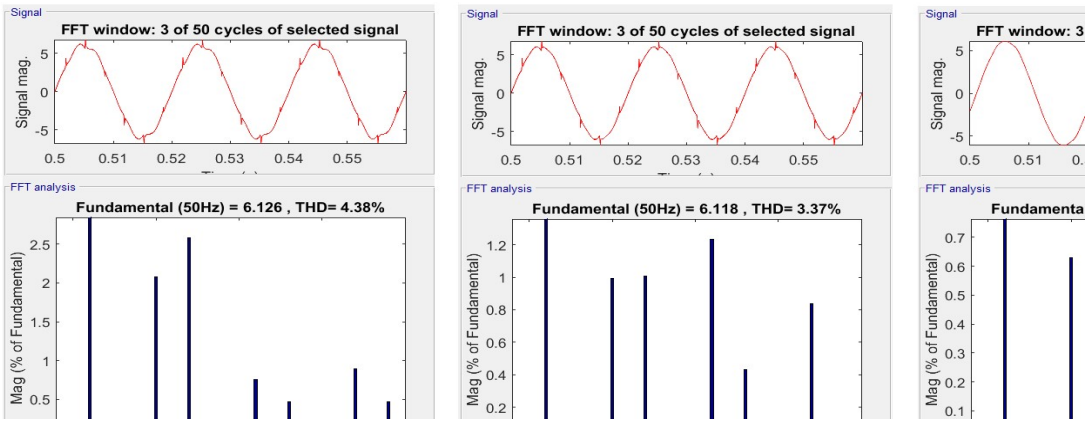

Figure 9: a) THD of source current with PI b) THD of source current with FOPI c) THD of source current with SMFO-PI

Table 1: THD comparison

Name of the parameter	No UPQC	PI	FOPI	SM-FOPI
Isabc	28.13	4.13%	3.25%	1.05%

V. CONCLUSION

The UPQC system was successfully designed and modeled using MATLAB SIMULINK. It has improved the receiving end voltage and provided time harmonics to the load. The UPQC system was simulated in closed loop with PI and FO-PID controllers, and the outcomes were given. In this work, an SMFOPI-based UPQC has been proposed to address power quality issues, specifically harmonic compensation and load voltage sag. The performance of the UPQC was demonstrated on a power distribution system consisting of nonlinear loads. The UPQC with SMFOPI controller was more capable of mitigating power quality issues compared to the UPQC with FOPI controller. The THD of the source current was reduced to 1.05% for the system operated with SMFOPI controller integrated UPQC.

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