Simulation analysis of electric vehicle battery charger with single phase AC supply

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Abstract—

A new zero voltage switching (ZVS) fnll-bridge DCDC converter for traction battery charging is proposed in this paper. The proposed isolated DC-DC converter is a part of ACDC converter in an electric vehicle charger. The main active switches in the converter turn-on at zero voltage over full-load range with the help of passive auxiliary circuit. The diode clamping circuit on the primary side eliminates the voltage spikes on the secondary rectifier diodes which are commonly present in conventional full-bridge DC-DC converters. The main switches are controlled with the proposed asymmetrical pulse width modulation (APWM) technique resulting in higher efficiency. APWM reduces the current stress of the main switches and the circulating losses by minimizing the auxiliary reactive current over the full-load range of DC-DC converter compared to conventional phase-shift modulation (PSM) method. The steadystate analysis of the converter is explained in detail with time intervals and respective governing analytical equations are provided. A 100kHz, full-bridge DC-DC converter is implemented on ORCAD/Pspice simulation platform and the ZVS results at full-load and light load, and secondary voltage result at full-load are presented. The advantage of APWM over PSM is also verified through the current stress results of the main switches at different loads for the proposed DC-DC converter.

Index Terms - Full-bridge DC-DC converter, traction battery charging, electric vehicle charger, zero voltage switching (ZVS).

I. INTRODUCTION

Plug-in electric vehicles (EVs) are the promising solution for nowadays transportation in view of reducing greenhouse gas emissions for human liveable and sustainable environment [1]. The high voltage traction battery in EVs is charged from utility grid by an EV charger [2]. The block diagram of a typical on-board EV charger power conditioning system is shown in Fig. 1. The two-stage AC-DC and DC-DC power conversion system provides inherent low frequency ripple rejection in the outut current. The font-end AC-DC power factor correction (PFC) stage converts the AC grid voltage to a regulated intermediate DC bus link voltage and improves the quality of input current at the same time. The second stage DC-DC converter converts DC bus link voltage to a regulated DC output voltage to charge the high voltage battery pack providing electrical isolation between grid supply and taction battery.

Full-bridge DC-DC converter topology [3] is preferred for second stage because of its high efficiency, high power density, high reliability, voltage gain and isolation capability. However, the conventional fll-bridge converter has the following disadvantages: loss of zero voltage switching (ZVS) during t-on at light loads, secondary duty cycle loss,

high circulating curent and high voltage spikes on outut rectifier diodes due to the leakage inductance of transformer and the exteral series inductance. Full-load range ZVS can be achieved by adding auxiliary current source network to the conventional fll-bridge converter. A single inductor auxiliary current source network is proposed in [4]-[5] to improve the ZVS range. However, the auxiliary current is not controlled which increases circulating and conduction losses. The passive adaptive auxiliary current source networks are proposed in [6][14] where the auxiliary reactive current is adaptive with respect to the load, i.e., it is minimum at full-load and progressively increased when the load is decreased. But, the drawback of these topologies is the higher auxiliary current especially at light loads which increases the circulating losses in the converter. To further minimize these circulating losses, the auxiliary current is controlled with active switches [15]-[16] which results in increased cost and complexity of the converter. The converter proposed in [17] eliminates the secondary voltage spikes with clamping diode network on primary. Similar primary clamping diode network is used in the proposed converter.

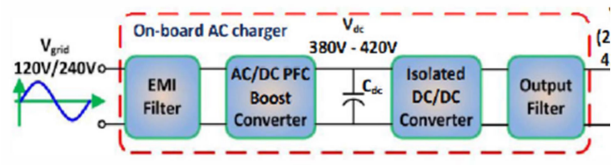

Fig. 1. Block diagram of on-board EV charger power conditioning system.

In this paper, a new full-bridge DC-DC converter with passive auxiliary circuit that offers ZVS for all main switches on primary side throughout the battery charging load range is proposed. It also eliminates the severe voltage spikes on the secondary rectifier diodes as the converter is integrated with clamping diode network on the primary side. The output voltage is controlled using asymmetrical pulse width modulation (AWM) technique. The proposed AWM gating technique ensures low current stress of the main active switches, reduced conduction losses and circulating losses during freewheeling period compared to conventional phase-shift modulation (PSM) resulting in increased efficiency.

The rest of the paper is organized as follows: In section II, the steady-state analysis of te proposed converter is presented. The simulation results for ZVS of main switches, the secondary voltage of main transformer and the current stress of main switches with AWM and PSM at different loads are presented in Section III. Finally, Section IV draws conclusion for the proposed ZVS APWM fll-bridge DC-DC converter and proposed APWM gating technique.

II. PFC BOOST CONVERTER

An active power factor corrector (active PFC) is a power electronic system that changes the waveshape of current drawn by a load to improve the power factor. The purpose is to make the load circuitry that is power factor corrected appear purely resistive (apparent power equal to real power). In this case, the voltage and current are in phase and the reactive power consumption is zero. This enables the most efficient delivery of electrical power from the power company to the consumer. An active PFC is a power electronic system that is designed to have control over the amount of power drawn by a load and in return it obtains a power factor as close as possible to unity. Commonly any active PFC design functions by controlling the input current of the load in order to make the current waveform follow the mains voltage waveform closely (i.e. a sine wave). A combination of the reactive elements and some active switches are in order to increase

the effectiveness of the line current shaping and to obtain controllable output voltage. [2] [3] In this paper a method of active power factor correction is proposed. It makes use of a boost converter.

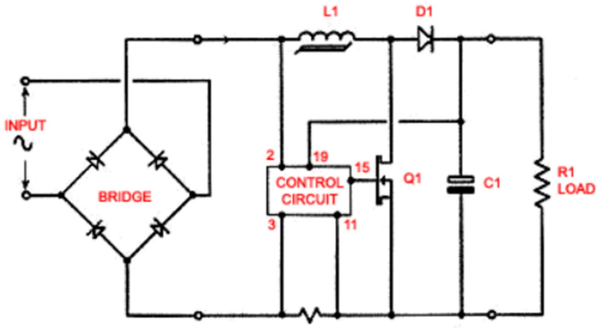

Figure 2: PFC boost circuit

A boost converter (step-up converter) is a DC-to-DC power converter with an output voltage greater than its input voltage. It is a class of switched-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element, a capacitor, inductor, or the two in combination. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple. It is a type of power converter in which the DC voltage obtained at the output stage is greater than that given at the input. It can be considered as a kind of switching-mode power supply (SMPS). Although it can be formed in different configurations, the basic structure must have at least two semiconductor switches (generally a diode and a transistor) and one energy storing element must be used.

The Boost converter has two distinct states:

- The On-state, in which the switch S is closed, and then there is a constant increase in the inductor current.
- The Off-state, in which the switch S is made open and the inductor current now flows through the diode D, the load R and the capacitor C. In this state, the energy that has been accumulated in the inductor gets transferred to the capacitor.

The input current and the inductor current are the same. Hence as one can see clearly that current in a boost converter is continuous type and hence the design of input filter is somewhat relaxed or it is of lower value.

The key principle that drives the boost converter is the tendency of an inductor to resist changes in current by creating and destroying a magnetic field. In a boost converter, the output voltage is always higher than the input voltage. A schematic of a boost power stage is shown in Figure 3.

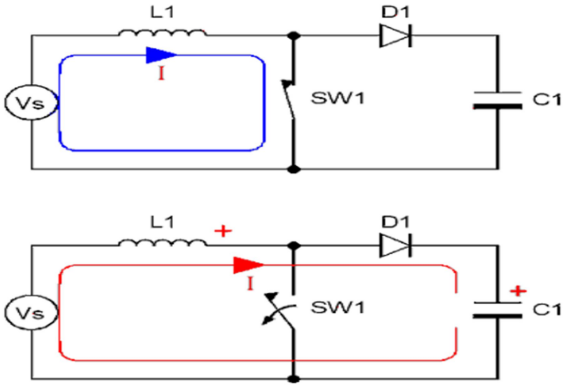

Figure 3: Two operating states of Boost Converter

III. ACTIVE FULLE BRIDGE AC-DC CONVERTER

The proposed ZVS APWM full-bridge DC-DC converter shown in Fig. 4(a) and the proposed AWM gating technique is shown in Fig. 4(b). The steady-state analysis of the proposed soft switched APWM full-bridge DC-DC converter over the operating range is explained in this section. The following assumptions are considered for ease of analysis.

• The switching elements are ideal.

• Resistance and inter-winding capacitance of the main power transformer Tr and auxiliary transformer T a are neglected.

• Magnetizing inductance of both the transformers Tr and T a is very high such that the magnetizing current is neglected.

• Resistance and winding capacitance of the series inductor and auxiliary inductor are neglected.

• The filter inductor is large enough such that the output current is constant.

• Capacitances across main switches are of equal values.

ZVS for all active switches and reduced circulating and conduction losses over the operating range is ensured by the proposed topology combined with the AWM gating technique as shown in Fig. 4(b).

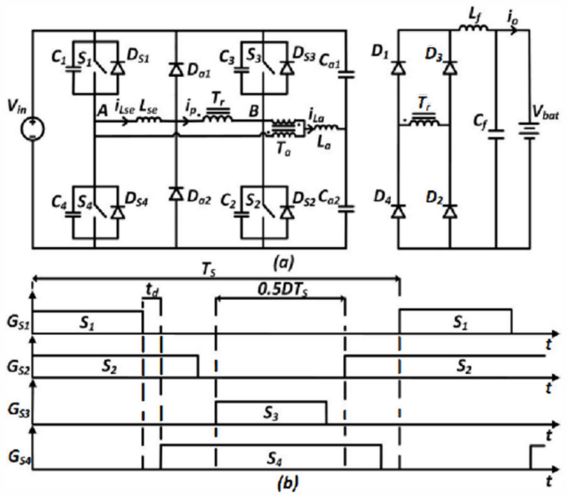

Fig. 4. (a) Proposed ZVS fll-bridge DC-DC converter. (b) Proposed AWM gating technique.

A. Interval 1

In this interval, the power is transferred from input source Vn to the load through the main switches SI and S2, and output rectifier diodes DI and D2 as shown in Fig. 5. During this interval,

$$v_{AB}(t) = V_{in}; v_{Tap}(t) = v_{Tas}(t) = \frac{V_{in}}{2} \quad (1)$$

$$i_{Lse}(t) = i_p(t) = nI_o \quad (2)$$

$$i_{La}(t) = I_{La}(t_0) + \frac{V_{in}(1-D)}{2L_a}(t-t_0) \quad (3)$$

$$i_{S1}(t) = nI_o + \frac{I_{LaP}}{4}; i_{S2}(t) = nI_o - \frac{I_{LaP}}{4} \quad (4)$$

where Vin is the input voltage, VAB(t is the inverter outut voltage, VTap(t) and VTa(t) are the voltages across primary and secondary of T a, hslt and ip(t are the series inductor and T r primary currents, 10 is the load current, haP is the peak value of auxiliary inductor current, and islt and iS2(t) are SI and S2 currents. This interval ends when the gating signal to the main switch SI is ted off.

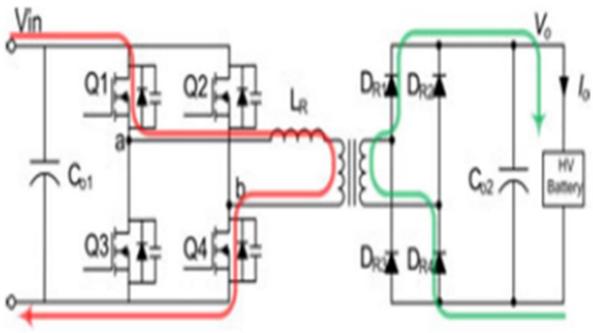

Figure 5.Equivalent circuit for Interval 1

B. Interval 2

During Interval 2 the current through the inductor LR does not reach zero on reaching the instant T2 and the rectifier diodes DR1 and DR4 are ON. At the end of this interval,

$$i(t) = i \qquad (5)$$

The equivalent circuit for this interval is as shown in the Fig.6.

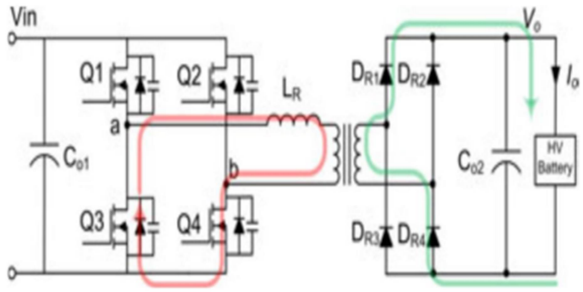

Figure 6:.Equivalent circuit for Interval 2

C.Interval 3

At T2, Q3 turns ON and Q4 turns OFF. This toggle time depends on the resonant delay that occurs prior to Q2 turning ON. When Q3 is ON and Q4 OFF, the inductor current which flows through Q4 finds an alternate path by charging/discharging the parasitic capacitances of switches Q4 and Q2 until the body diode of Q2 is forward biased. Switch Q2 can be turned ON with ZVS if the resonant delay is properly set. At T3 the complete energy stored in is transmitted to the output and the current becomes zero and the rectifier diodes DR1 and DR4 turn OFF. The resonant inductor current.

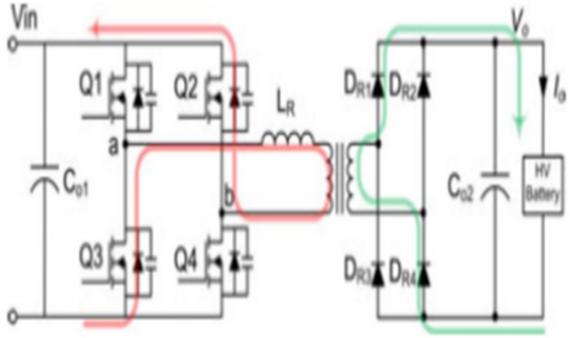

Figure 7:.Equivalent circuit for Interval 3

D. Interval 4

In interval 4, switches Q2 and Q3 are ON and Q1 and Q4 are OFF. The primary current flows through Q2, inductor LR, transformer primary and Q3. The rate of increase of the current (di/dt)) through LR is proportional to the difference between the input voltage Vin and the output voltage Vo. In this mode power is transferred to the output through output diodes DR2 and DR3 and moreover energy is stored in LR. The equivalent circuit for this interval is as shown in the Fig.8.

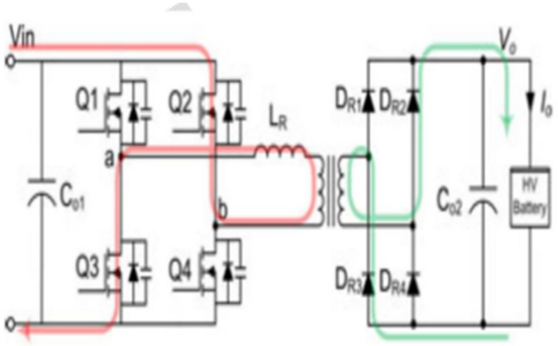

Figure 8:.Equivalent circuit for Interval 4

E. Interval 5

During Interval 5 the current through the resonant inductor does not reach zero and the rectifier diodes DR3 and DR4 are ON. The

equivalent circuit for this mode is shown in Fig.9.

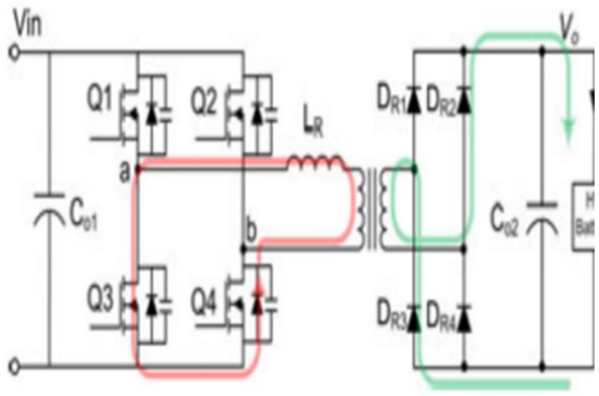

Figure 9:.Equivalent circuit for Interval 5

F. Interval 6

This interval is the negative equivalent of the interval 3 as shown in Fig.10.

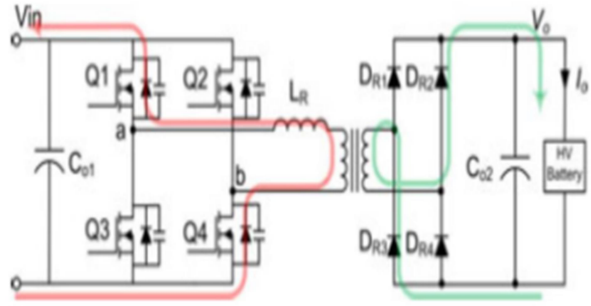

Figure 10.Equivalent circuit for Interval 6

IV. SIMULATION RESULTS

In this section, simulation results for zero voltage switching of main active switches, ripple fee Tr secondary voltage and current stress comparison of the main active switches with APWM and PSM techiques at different battery charging loads are presented for the proposed fll-bridge converter. The fll-bridge converter is rated at 1.65kW with an input/outut voltage of 400V1240V-420V operating at switching fequency 100kHz. The circuit parameters are set as follows: Lse = 101H, La = 61H, Lf= 3mH, Cal = Co2 = 51F, Cf= 101F.

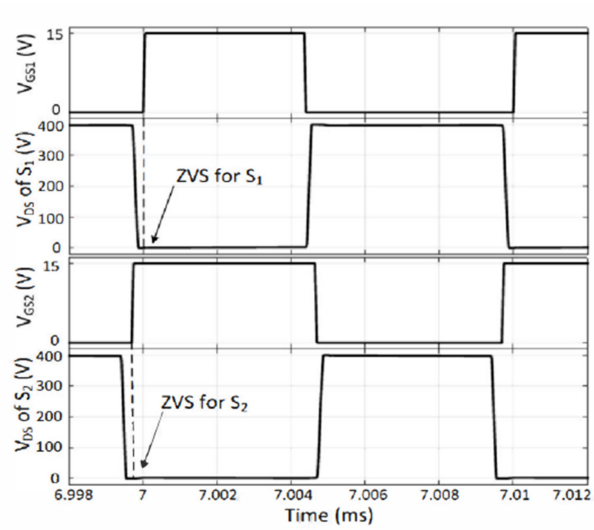

Fig. 11. ZVS for main switches SI and S2 at fll-load (402V, 4.IA)

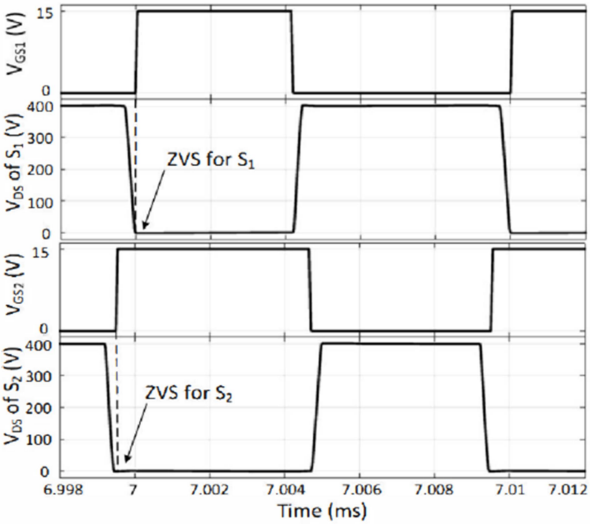

Fig. 12. ZVS for main switches SI and S2 at light load (405V, O.4IA)

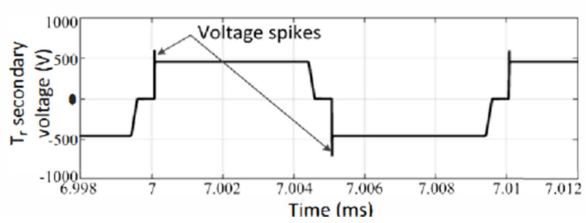

Fig. 13. Transformer Tr secondary voltage without clamp circuit (402V, 4.IA)

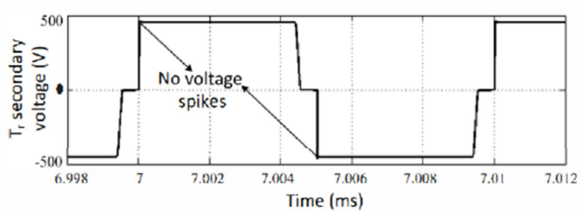

Fig. 14. Transformer T, secondary voltage at fll-load (402V, 4.IA)

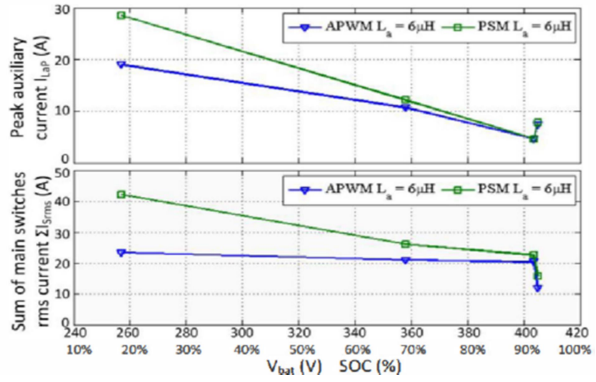

Fig. 15: Pea auxiliary current (top) and sum of all active switches SI-S4

R.M.S. current (bottom) at different loads with AW and PSM. The proposed fll-bridge DC-DC converter topology is simulated with the proposed AWM gating scheme at fll load (1.65kW) and light load (10% of fll-load) conditions. The respective gating signal and drain to source voltage for the active switches S1, S2 are shown in Fig. 6 and Fig. 7 at full - load and light load conditions respectively. It can be seen from these figures that the voltage across the switches becomes zero before the gating signal is applied, i.e., the active switches SI, S2 are ted on with ZVS as explained in Interval 12 and Interval 5 respectively. Similarly, ZVS for S3 and S4 can be achieved as explained in Interval 4 and Interval 2 respectively. The secondary voltage of the main transformer Tr is shown in Fig. 14 without clamp diode network and Fig. 14 for the proposed converter. It can be observed from Fig. 15 that the voltage spikes on both positive and negative voltage sides are eliminated as explained in Interval 5 and Interval 10-12. The peak auxiliary current haP and the sum of all active switches SI-S4 r.m.s currents () at different loads with APWM and PSM are simulated and the results are shown in Fig. 15. The results show that the APWM is better than PSM as the magnitude of hap is small and the current stress is less which results in improved efficiency of converter.

V. CONCLUSION

The project presents an electric vehicle battery charger using an improved ZVS full bridge dc–dc converter with capacitive output filter. The detailed operating intervals were considered and the simulation results were examined. The input power factor with and without PFC has been discussed and compared. The second stage of the proposed charger attains soft switching for the full-bridge primary switches, clamps the voltage across the output rectifier to the output voltage and the current through the rectifier diodes has a low (di/dt) which helps to reduce reverse recovery losses.

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